## REMARKS

Claims 34-37 and 42-45 are pending in the present application. In the Office Action dated August 4, 2005, claims 34, 36-37, and 44-45 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,086,018 to Conru et al. ("Conru"). Claims 35, 38-41 and 46-49 were rejected under 35 U.S.C. 103(a) as being unpatentable over Conru. Claim 42 was rejected under 35 U.S.C. 103(a) as being unpatentable over Conru in view of U.S. Patent No. 6,266,249 to Desai et al. ("Desai").

The embodiments disclosed in the present application will now be discussed in comparison to the cited references. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the cited references, does not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

Embodiments of the invention are directed to Board-on-Chip ("BOC") and Lead-on-Chip ("LOC") semiconductor packages attached with an adhesive die attach material that is cured through simultaneous application of uniform pressure and heat. One problem encountered when attaching dies to substrates with adhesives is that voids may form at the die attach bondline. The die attach bondline is the interface between the surfaces of the die and/or substrate on the one hand, and the adhesive on the other. Voids form in the adhesives during the heating process when moisture or contaminants present on the die attach bondline vaporize and create a bubble (or void) within the adhesive.

Embodiments of the invention are directed to semiconductor device packages having bondlines formed of adhesives cured in a chamber, such as an autoclave, with simultaneous application of heat and uniform pressure. The controlled temperature and pressure within the autoclave melt the adhesive, while increasing the vaporization point of any contaminants present at the die attach bondline. Thus, the bondline of the resultant semiconductor package assembly has a substantially void free bondline, particularly when compared to the amount of voids present in the bondlines of adhesive die attach materials cured by conventional processes.

Conru describes a lead-on-chip semiconductor package having leads 14 attached to a die 12 by strips of adhesive 11. A substrate 18 is further attached over the leads 14 with an adhesive layer 17 intermediate the substrate and the leads 14. A platen applies heat and force to the substrate 18 and adhesive 17 to soften the adhesive 17 and force it between the lead frame members and around the wires. Conru makes clear that the platen exerts mechanical pressure on the substrate, which must be sufficient to flatten the wires 16 against their respective bond pads and leads to which the wires are connected. Conru does not teach a semiconductor package assembly having a substantially void free bondline. The process of using a platen to apply mechanical pressure to the substrate disclosed in Conru does not appear to result in the application of uniform pressure and heat. Thus, the process of using a platen to apply mechanical pressure on the substrate disclosed in Conru does not appear to result in a die attach bondline having few or no voids. In fact, Conru is silent with respect voids at the die attach bondline and does recognize the problems associated with them.

Desai does not remedy any of the deficiencies of Conru.

Turning now to the claims, the patentably distinct differences between the cited references and the claim language will be specifically pointed out. Amended claim 34 recites, in part, "adhesive die attach material disposed between the semiconductor die and the substrate, the adhesive die attach material directly abutting the substrate and the semiconductor, a die attach bondline at the interface between the adhesive die attach material and the semiconductor die being substantially void free." Neither Conru nor Desai disclose or fairly suggest a die attach bondline at the interface between the adhesive die attach material and the semiconductor die having substantially no voids. Conru does not expressly teach such a substantially void free structure and the process disclosed in Conru does not appear to result in such a structure.

Amended claim 42 recites, in part, "a die attach bondline at the interface between the semiconductor die and the first surface of the substrate being substantially void free." Again, neither Conru nor Desai disclose or fairly suggest a die attach bondline at the interface between the adhesive die attach material and the semiconductor die having substantially no voids. Conru does not expressly teach such a substantially void free structure and the process disclosed in Conru does not appear to result in such a structure.

Claims depending from claims 34 and 42 are also allowable due to depending from an allowable base claim and further in view of the additional limitations recited in the dependent claims.

All of the claims remaining in the application (claims 34-37 and 42-45) are now clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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